REMARKS

The Examiner objected claims 6 and 8-11 as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Applicants thank the Examiner and rewrote claims 6 and 8 in independent form.

The Examiner rejected claims 1, 3, 7 and 12-14 under 35 U.S.C. § 102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050).

The Examiner rejected claims 1 and 7 under 35 U.S.C. § 102(e) as allegedly being anticipated by Takao (US 2004/0137701).

The Examiner rejected claims 2 and 4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Takao as above in view of Chae *et al.* (US 6,958,312).

The Examiner rejected claim 5 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ference as above in view of Kawakami (US 2003/0190795).

Applicants respectfully traverse the § 102 and § 103 rejections with the following arguments.

35 U.S.C. §102

The Examiner rejected claims 1, 3, 7 and 12-14 under 35 U.S.C. § 102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050).

Applicants respectfully contend that Ference does not anticipate claim 1, because Ference does not teach each and every feature of claim 1. For example, Ference does not teach "forming N interconnect layers ... wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region, wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and wherein the entire **continuous** etchable block comprises **essentially a same material throughout the entire continuous etchable block,**" in step (c) of claim 1 (bold emphasis added).

More specifically, the Examiner argues in bullet # 2 of the Office Action that the interconnect layer 22 and the additional intermediate conductive layers in column 5, lines 7-10 of Ference may be used to represent the N interconnect layers of claim 1. In response, Applicants note that Ference does not teach the relative position between these N interconnect layers of claim 1. More specifically, Ference does not teach that interconnect layer 22 and the additional intermediate conductive layers are in direct physical contact with one another so that the etchable portions of these layers form a **continuous** etchable block. Even if the etchable portions of these layers formed a **continuous** etchable block, Ference does not teach that this continuous etchable block comprises **essentially a same material throughout the entire continuous etchable block** as claimed in claim 1.

In contrast, in claim 1, the etchable block is a **continuous** one. In other words, the N interconnect layers are in direct physical contact with one another. More over, in claim 1, the continuous etchable block comprises **essentially a same material throughout the entire continuous etchable block.** Therefore, claim 1 is not anticipated by Ference.

Based on the preceding arguments, Applicants respectfully maintain that Ference does not anticipate claim 1, and that claim 1 is in condition for allowance.

The Examiner rejected claims 3 and 7 under 35 U.S.C. §102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050). Since claims 3 and 7 depend from claim 1, which is not anticipated by Ference as argued above, Applicants contend that claims 3 and 7 are likewise in condition for allowance.

Applicants respectfully contend that Ference does not anticipate claim 12, because Ference does not teach each and every feature of claim 12. For example, Ference does not teach "forming N interconnect layers ... wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region, wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and wherein the entire **continuous** etchable block comprises **essentially a same material throughout the entire continuous etchable block,**" in step (c) of claim 12 (bold emphasis added).

More specifically, the Examiner argues in bullet # 2 of the Office Action that the interconnect layer 22 and the additional intermediate conductive layers in column 5, lines 7-10 of Ference may be used to represent the N interconnect layers of claim 12. In response, Applicants note

that Ference does not teach the relative position between these N interconnect layers of claim 12. More specifically, Ference does not teach that interconnect layer 22 and the additional intermediate conductive layers are in direct physical contact with one another so that the etchable portions of these layers form a **continuous** etchable block. Even if the etchable portions of these layers formed a **continuous** etchable block, Ference does not teach that this continuous etchable block comprises **essentially a same material throughout the entire continuous etchable block** as claimed in claim 12.

In contrast, in claim 12, the etchable block is a **continuous** one. In other words, the N interconnect layers are in direct physical contact with one another. More over, in claim 12, the continuous etchable block comprises **essentially a same material throughout the entire continuous etchable block**. Therefore, claim 12 is not anticipated by Ference.

Based on the preceding arguments, Applicants respectfully maintain that Ference does not anticipate claim 12, and that claim 12 is in condition for allowance.

The Examiner rejected claims 13 and 14 under 35 U.S.C. §102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050). Since claims 13 and 14 depend from claim 12, which is not anticipated by Ference as argued above, Applicants contend that claims 13 and 14 are likewise in condition for allowance.

The Examiner rejected claims 1 and 7 under 35 U.S.C. § 102(e) as allegedly being anticipated by Takao (US 2004/0137701).

Applicants respectfully contend that Takao does not anticipate claim 1, because Takao does not teach each and every feature of claim 1. For example, Takao does not teach the feature "forming N interconnect layers ... wherein each layer of the N interconnect layers comprises an

etchable portion directly above the semiconductor border region, wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and wherein the entire **continuous** etchable block comprises **essentially a same material throughout the entire continuous etchable block,**" in step (c) of claim 1 (bold emphasis added).

More specifically, if the layers 18, 19 and 30 in Fig. 5 of Takao were considered interconnect layers for the purpose of anticipating claim 1, their etchable portions would not form a continuous etchable block which comprises **essentially a same material throughout the entire continuous etchable block** as claimed in claim 1. This is because the layers 18, 19 and 30 comprise different materials (paragraphs 59, 60, and 61). Therefore, claim 1 is not anticipated by Takao.

Based on the preceding arguments, Applicants respectfully maintain that Takao does not anticipate claim 1, and that claim 1 is in condition for allowance.

The Examiner rejected claim 7 under 35 U.S.C. §102(b) as allegedly being anticipated by Takao *et al.* (US 2004/0137701). Since claim 7 depends from claim 1, Applicants contend that claim 7 is likewise in condition for allowance.

The Examiner objected claims 6 and 8-11 as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, Applicants thank the Examiner and rewrote claims 6 and 8 in independent form.

35 U.S.C. §103

The Examiner rejected claims 2 and 4 under 35 U.S.C. §103(a) as allegedly being unpatentable over Takao et al. (US 2004/0137701) in view of Cohen (US 6,903,016). Since claims 2 and 4 depend from claim 1, which is in condition for allowance as argued above, Applicants contend that claims 2 and 4 are likewise in condition for allowance.

The Examiner rejected claim 5 under 35 U.S.C. §103(a) as allegedly being unpatentable over Ference et al. (US 6,611,050) in view of Kawakami (US 2003/0190795). Since claim 5 depends from claim 1, which is in condition for allowance as argued above, Applicants contend that claim 5 is likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicant's representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Date: February 07, 2006

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